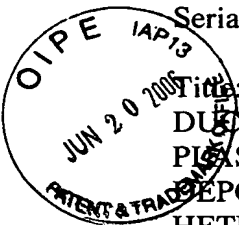


In the United States Patent and Trademark Office



Serial No.: 10/550,855

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Filing Date:

Title: FORMATION OF THIN SEMICON-
DUCTOR LAYERS BY LOW-ENERGY
PLASMA ENHANCED CHEMICAL VAPOR
DEPOSITION AND SEMICONDUCTOR
HETEROSTRUCTURE DEVICES

Examiner:

Art Unit: 1734

Applicant: VON KAENEL, Hans

Atty docket No: PUS-E005-013

INFORMATION DISCLOSURE STATEMENT

To: U.S. Patent and Trademark Office
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Randolph Building
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Dear Sir,

Pursuant to the provisions of 37 C.F.R. §1.97, Applicant encloses the references set forth in the attached modified form PTO/SB/O8A. No inference should be made that the cited references are in fact material, are in fact prior art, are analogous art, or that no better art exists. The cited patents are listed in numerical order and not in any order based on their pertinence.

It is requested that the Examiner fully consider the cited references and that they be cited on the front of any patent issuing from this application.

An early action on the merits is respectfully requested.

If the Examiner has further questions, he is invited to contact the undersigned at phone 011-4171 230 1000, fax at 011-4171 230 1001 or e-mail at sherman@patentinfo.net.

Respectfully submitted,

Sherman D. PERNIA
U.S. Reg. No. 34,404

Date: 15 June 2006

Enclosures: IDS form
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	4
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Complete if Known

Application Number	10/550,855
Filing Date	
First Named Inventor	VON KAENEL, Hans
Art Unit	1734
Examiner Name	
Attorney Docket Number	PUS-E005-013

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			
		EP 1 315 199	05/28/2003	VON KAENEL	entire document	
		WO/1998/058099	12/23/1998	VON KAENEL et al.	entire document	
		WO/2003/044839	05/30/2003	VON KAENEL	entire document	

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		Application Number	10/550,855
		Filing Date	
		First Named Inventor	VON KAENEL, Hans
		Art Unit	1734
		Examiner Name	
Sheet 2	of 4	Attorney Docket Number PUS-E005-013	

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	1	KASPER et al., New virtual substrate concept for vertical MOS transistors, Thin Solid Films, Vol. 336, p. 319-22 (1998)	
	2	BAUER et al., Relaxed SiGe buffers with thicknesses below 0.1 um, Thin Solid Films, Vol. 369, p. 152-56 (2000)	
	3	HACKBARTH et al., Alternatives to thick MBE-grown relaxed SiGe buffers, Thin Solid Films, Vol. 369, p. 148-51 (2000)	
	4	UENO et al., Low temperature buffer growth for modulation doped SiGe/Ge/SiGe heterostructures with high hole mobility, Thin Solid Films, Vol. 369, p. 320-23 (2000)	
	5	KUCHENBECKER et al., Thin SiGe buffer layer growth by in situ low energy hydrogen plasma preparation, Thin Solid Films, Vol. 389, p. 146-52 (2001)	
	6	FITZGERALD et al., Totally relaxed GeXSi1-X layers with low threading dislocation densities grown on Si substrates, Appl. Phys. Lett., Vol. 59, p. 811-13 (1991)	
	7	ISMAIL et al., Extremely high electron mobility in Si/SiGe modulation-doped heterostructures, Appl. Phys. Lett., Vol. 66, p. 1077-79 (1995)	
	8	LINDER et al., Reduction of dislocation density in mismatched SiGe/Si using a low-temperature Si buffer layer, Appl. Phys. Lett., Vol. 70, p. 3224-26 (1997)	
	9	LI et al., Relaxed Si0.7Ge0.3 layers grown on low-temperature Si buffers with low threading dislocation density, Appl. Phys. Lett., Vol. 71, p. 3132-34 (1997)	
	10	PENG et al., Relaxed Ge0.9Si0.1 alloy layers with low threading dislocation densities grown on low-temperature Si buffers, Appl. Phys. Lett., Vol. 72, p. 3160-62 (1998)	

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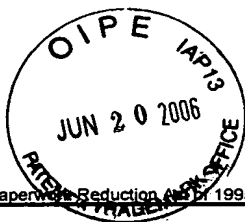
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		Examiner Name	
Sheet 3	of 4	Attorney Docket Number	PUS-E005-013

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	11	ROSENBLAD et al., A plasma process for ultrafast deposition of SiGe graded buffer layers, Appl. Phys. Lett., Vol 76, p. 427-29 (2000)	
	12	VON KAENEL et al., Very high hole mobilities in modulation-doped Ge quantum wells grown by low-energy plasma enhanced chemical vapor deposition, Appl. Phys. Lett., Vol. 80, p. 2922-24 (2002)	
	13	MUROTA et al., Low-Temperature Epitaxial Growth of Si/Si1-XGeX/Si Heterostructure by Chemical Vapor Deposition, Jpn. J. Appl. Phys., Vol. 33, p. 2290-99 (1994)	
	14	CHEN et al., Low-temperature buffer layer for growth of a low-dislocation-density SiGe layer on Si by molecular-beam epitaxy, J. Appl. Phys., Vol. 79, p. 1167-69 (1996)	
	15	WEITZ et al., Tilted magnetic field studies of spin- and valley-splittings in Si/Si1-XGeX heterostructures, Surf. Sci., Vol. 361/362, p. 542-46 (1996)	
	16	SCHUEGRAF et al., Handbook of thin-film deposition processes and techniques, Noyes Publications, New Jersey, US, p. 26-79 article by M.L. HAMMOND (1988)	
	17	MANTL et al., Strain relaxation of epitaxial SiGe layers on Si(100) improved by hydrogen implantation, Nucl. Instr. and Meth. in Phys. Res., Vol. B 147, p. 29-34 (1999)	
	18	HOLLAENDER et al., Enhanced strain relaxation of epitaxial SiGe layers on Si(100) after H+ ion implantation, Nucl. Instr. and Meth. in Phys. Res., Vol. B 148, p. 200-05, (1999)	

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First Named Inventor	VON KAENEL, Hans
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Attorney Docket Number	PUS-E005-013

Sheet 4

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	19	HOLLAENDER et al., Strain relaxation of pseudomorphic Si1-XGeX/Si(100) heterostructures after hydrogen or helium ion implantation for virtual substrate fabrication, Nucl. Instr. and Meth. in Phys. Res., Vol. B 175-177, p. 357-67 (2001)	
	20	HERZOG et al., Si/SiGe n-MODFETs on Thin SiGe Virtual Substrates Prepared by Means of He Implantation, IEEE Electron Device Letters, Vol. 23, p. 485-87 (2002)	
	21	LYUTOVICH et al., Thin SiGe buffers with high Ge content for n-MOSFETs, Materials Science and Engineering, Vol. B89, p. 341-45 (2002)	

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